# (12) EUROPEAN PATENT APPLICATION

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(54) DMA controller

(57) Address generators output addresses of transfer data of transfer origin and destination DRAM's. Updating of the transfer addresses from the address generators during execution of DMA is performed based on a CAS signal from a timing signal generator. A delay element delays the CAS signal by a time which is the sum of an access time of the transfer origin DRAM and a data set-up time of the transfer destination DRAM. A transfer data counter counts the number of leading edges of the CAS signal while a RAS signal from the timing signal generator is held active. When a counted value reaches a preset value, the transfer data counter outputs continuous data transfer suspension information to the timing signal generator. With this arrangement, the halt in operation of a CPU due to continuous occupation of a bus is effectively prevented while achieving the increased data transfer rate.

FIG. 4
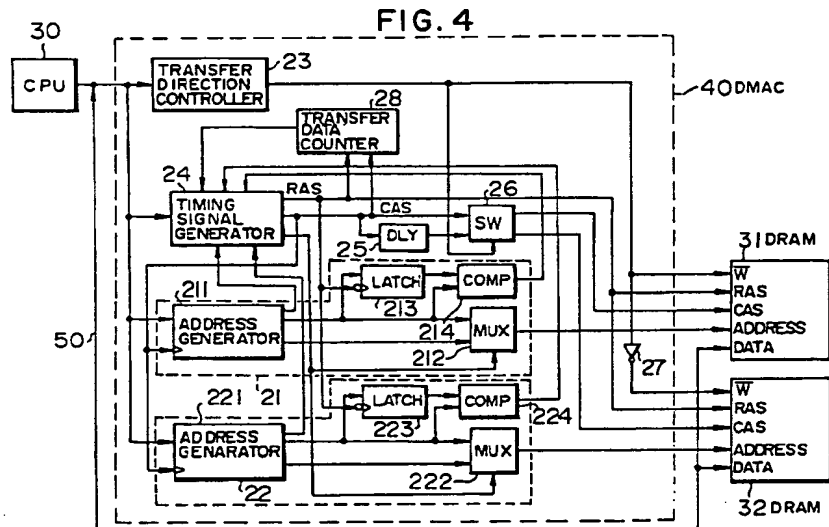
EP 0 735 491 A2

operation of a CPU 30 is stopped while the bus 50 is occupied.

The present invention has been made in view of the foregoing and has an object to provide a DMA controller which simultaneously achieves the continuous access and the simultaneous execution of reading and writing so as to further increase the data transfer rate while preventing an operation of a CPU from stopping due to continuous occupation of a bus.

In order to accomplish the foregoing object, a DMA controller according to the present invention comprises a first memory control section for producing, by a first address generator, a first address signal for a first memory which is a transfer origin and continuously accessible, and for outputting the first address signal to the first memory; a second memory control section for producing, by a second address generator, a second address signal for a second memory which is a transfer destination and continuously accessible, and for outputting the second address signal to the second memory; a timing signal generator for producing first and second address strobe signals based on output control signals from the first and second memory control sections, the timing signal generator outputting the first address strobe signal to the first and second memories, respectively, and the second address strobe signal to the first memory; delay means for delaying the second address strobe signal by a time which is a sum of an access time of the first memory and a data set-up time of the second memory, and for outputting the delayed second address strobe signal to the second memory; first and second control means, provided in the first and second memory control sections, respectively, for outputting control signals separately to the timing signal generator so as to control generation of the first and second address strobe signals for achieving continuous access of the first and second memories independently of each other; and a transfer data counter for counting the number of transfer data from the second address strobe signal of the timing signal generator and for outputting transfer suspension information to the timing signal generator when a counted value reaches a preset value.

It may be arranged that the DMA controller further comprises transfer direction control means for subjecting the first memory to a reading control and the second memory to a writing control, and switching means, based on an output signal from the transfer direction control means, for feeding the second address strobe signal from the timing signal generator to the first memory and for feeding the delayed second address strobe signal from the delay means to the second memory. With this arrangement, a direction of the data transfer between the two memories can be switched depending on an instruction from a senior device.

It may be arranged that at least one of the first and second memories is a dynamic random access memory which is operable in a page mode or a static column mode, and that each of the first and second control means includes latch means for holding a row address

in address signals outputted from corresponding one of the first and second address generators upon transition of the first address strobe signal to an active state at the time of starting the data transfer, and a comparator for comparing an output of the latch means and a row address in the address signals outputted from the corresponding one of the first and second address generators and for outputting a result of the comparison as the control signal to the timing signal generator, wherein, while the comparison result shows agreement, the timing signal generator controls the second address strobe signal to change alternately between active and inactive states while holding the first address strobe signal to be active. This arrangement is preferable in view of achieving the continuous access.

According to one aspect of the present invention, by repeating the writing of data, which are outputted by the first memory in synchronism with the second address strobe signal from the timing signal generator, into the second memory in synchronism with the delayed second address strobe signal, the first and second memories can be continuously accessed, and simultaneously, the data reading from the first memory and the data writing into the second memory can be achieved in one cycle.

According to another aspect of the present invention, the number of transfer data is counted by the transfer data counter, and when this counted value reaches the preset value, the first address strobe signal is forcibly set inactive based on the transfer suspension information. Thus, the number of continuous transfer data in the DMA transfer is limited to the foregoing preset value.

The present invention will be understood more fully from the detailed description given hereinbelow, taken in conjunction with the accompanying drawings.

In the drawings:

Fig. 1 is a block diagram showing a structure of a conventional DMA controller;
Fig. 2 is a block diagram showing a structure of another conventional DMA controller;
Fig. 3 is a block diagram showing a structure of a DMA controller previously proposed by the present inventors;
Fig. 4 is a block diagram showing a structure of a DMA controller according to a preferred embodiment of the present invention;
Fig. 5 is a timing chart for explaining an operation of the preferred embodiment of the present invention shown in Fig. 4;
Fig. 6 is a timing chart for explaining an operation of a page mode read cycle;
Fig. 7 is a timing chart for explaining an operation of a page mode write cycle;
Fig. 8 is a timing chart for explaining an operation of a static column mode read cycle; and
Fig. 9 is a timing chart for explaining an operation of a static column mode write cycle.

active and inactive states alternately, column addresses in the same row are inputted in sequence so that input data DQ1 to DQ4 are written in sequence. At this time, the output enable signal OE may be set in either of active and inactive states.

Now, the operation of this preferred embodiment will be described also referring to Fig. 5. First, before starting the data transfer, the CPU 30 sets the direction of the data transfer between the DRAM's 31 and 32 in the transfer direction controller 23, and further sets a transfer start address and a transfer termination address or the number of transfer data in the address generators 211 and 221. When the data transfer is performed in a direction from the DRAM 31 to the DRAM 32, the CPU 30 controls the output control signal of the transfer direction controller 23 to be at a high level.

The control signal outputted from the transfer direction controller 23 is fed to a write control terminal of the DRAM 31. Since the DRAM 31 is set to be subjected to a read control when the control signal from the transfer direction controller 23 is at a high level, the DRAM 31 works as the transfer origin DRAM. On the other hand, since the control signal from the transfer direction controller 23 is inverted via the inverter 27 and then inputted to a write control terminal of the DRAM 32, the DRAM 32 is subjected to a write control as opposed to the DRAM 31 so that the DRAM 32 works as the transfer destination DRAM. As appreciated, the foregoing transfer direction is reversed when the control signal from the transfer direction controller 23 is at a low level.

Then, the CPU 30 instructs the timing signal generator 24 to start the data transfer. In response to the data transfer start instruction from the CPU 30, the timing signal generator 24 switches the MUX's 212 and 222 to output the row addresses. Subsequently, as shown at (A) in Fig. 5, the timing signal generator 24 causes the RAS signal to fall at a time t1 so that the latch circuits 213 and 223 latch the foregoing row addresses, respectively. Thereafter, the timing signal generator 24 switches the MUX's 212 and 222 to output the column addresses.

Then, the timing signal generator 24 causes the CAS signal to fall at a time t2. Since the CAS signal is inputted as it is via the switching circuit 26 to the transfer origin DRAM in the DRAM's 31 and 32, the data is outputted from the transfer origin DRAM due to the falling of the CAS signal. This CAS signal is shown at (B) in Fig. 5. As shown at (E) in Fig. 5, the effective data is outputted from a time t3, that is, after a lapse of an access time from the falling of the CAS signal at the time t2.

On the other hand, since the CAS signal delayed by the given time via the delay circuit 25 is inputted via the switching circuit 26 to the transfer destination DRAM in the DRAM's 31 and 32, the data outputted from the transfer origin DRAM is written in the transfer destination DRAM due to the falling of this delayed CAS signal. This delayed CAS signal is shown at (C) in Fig. 5. Due to the delay achieved by the delay circuit 25, the transfer destination DRAM writes in the effective data immedi-

ately after the time t3. The data inputted to the transfer destination DRAM is shown at (F) in Fig. 5.

After the delayed CAS signal to the transfer destination DRAM shown at (C) in Fig. 5 is caused to fall and then a sufficient time for writing the data in the transfer destination DRAM elapses, the timing signal generator 24 raises the CAS signal as shown at (B) in Fig. 5. At this time, if the transfer termination address or the number of transfer data set in the address generators 211 and 221 by the CPU 30 is reached, the timing signal generator 24 raises the RAS signal so as to terminate the continuous access between the DRAM's 31 and 32.

Further, when a counter value of the transfer data counter 28, which counts the number of leading edges of the CAS signal (the number of transfer data), reaches the preset value, the timing signal generator 24 also raises the RAS signal based on the transfer suspension data outputted from the transfer data counter 28 to the timing signal generator 24, so as to terminate the continuous access between the DRAM's 31 and 32.

On the other hand, if the transfer termination address or the number of transfer data set in the address generators 211 and 221 by the CPU 30 is not reached and if the counter value of the transfer data counter 28 does not reach the preset value, the address generators 211 and 221 update the addresses fed to the address terminals of the DRAM's 31 and 32 at the time of rising of the CAS signal.

After this address updating, if the comparators 214 and 224 output detection signals indicative of coincidence of the row addresses, respectively, the timing signal generator 24 causes the CAS signal to fall so that the subsequent data transfer is achieved in the same manner as described above. Fig. 5 at (D) shows the addresses inputted to each of the DRAM's 31 and 32 via the MUX's 212 and 222.

As described above, the operation to perform the page mode access by repeatedly changing the CAS signal between the low level and the high level while the RAS signal is held at the low level, is repeated until the output of the comparator 214 or 224 indicates disagreement of the row addresses or the transfer termination address or the number of transfer data set in the address generator 211 or 221 is reached after the address updating of the address generators 211 and 221.

If the output of either the comparator 214 or the comparator 224 shows the disagreement or the counter value of the transfer data counter 28 reaches the preset number of transfer data, the timing signal generator 24 raises the RAS signal to suspend the continuous access to the DRAM's 31 and 32 and switches the MUX's 212 and 222 to output a row address in the same manner as that performed in response to the transfer start instruction from the CPU 30, so as to repeat the foregoing operation.

As described above, according to this preferred embodiment, since the continuous access based on the page mode of the DRAM's 31 and 32 and the execution

2. The DMA controller according to claim 1, further comprising transfer direction control means for subjecting said first memory to a reading control and said second memory to a writing control, and switching means, based on an output signal from said transfer direction control means, for feeding said second address strobe signal from said timing signal generator to said first memory and for feeding said delayed second address strobe signal from said delay means to said second memory.

3. The DMA controller according to claim 1 or 2, each of said first and second control means includes latch means for holding a row address in address signals outputted from corresponding one of said first and second address generators upon transition of said first address strobe signal to an active state at the time of starting the data transfer, and a comparator for comparing an output of said latch means and a row address in the address signals outputted from the corresponding one of said first and second address generators and for outputting a result of the comparison as said control signal to said timing signal generator,

wherein, while said comparison result shows agreement, said timing signal generator controls said second address strobe signal to change alternately between active and inactive states while holding said first address strobe signal to be active.

4. The DMA controller according to claim 1, 2, or 3, wherein said transfer data counter counts the number of transitions from active to inactive of said second address strobe signal while said first address strobe signal is held active and compares its counted value with said preset value.

5. The DMA controller according to any of claims 1 to 4, wherein each of said first and second memories is a dynamic random access memory which is operable in a page mode, and wherein said first address strobe signal is a row address strobe signal and said second address strobe signal is a column address strobe signal.

6. The DMA controller according to any of claims 1 to 5, wherein at least one of said first and second memories is a dynamic random access memory which is operable in a static column mode, and wherein said first address strobe signal is a row address strobe signal and said second address strobe signal is a chip select signal.
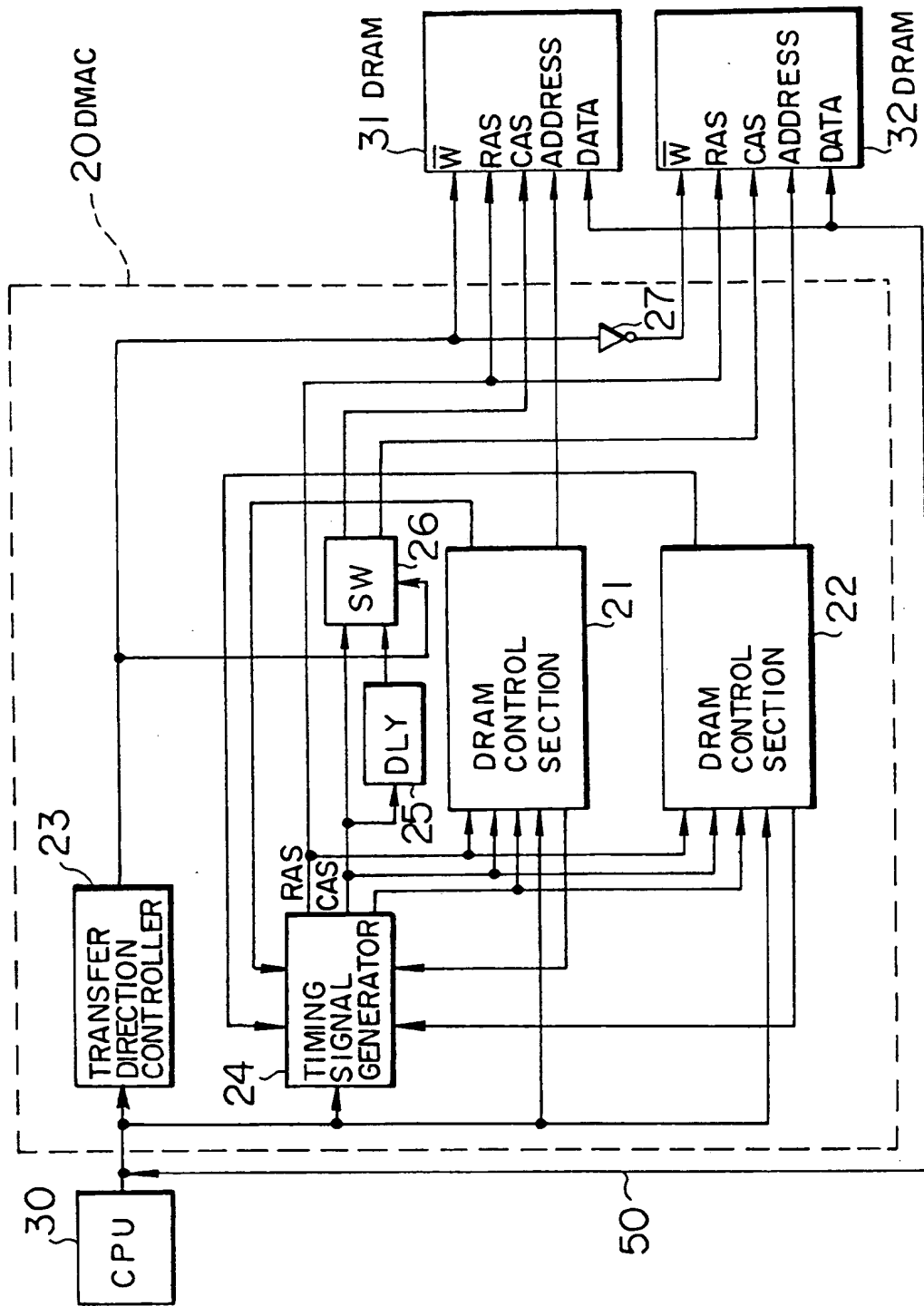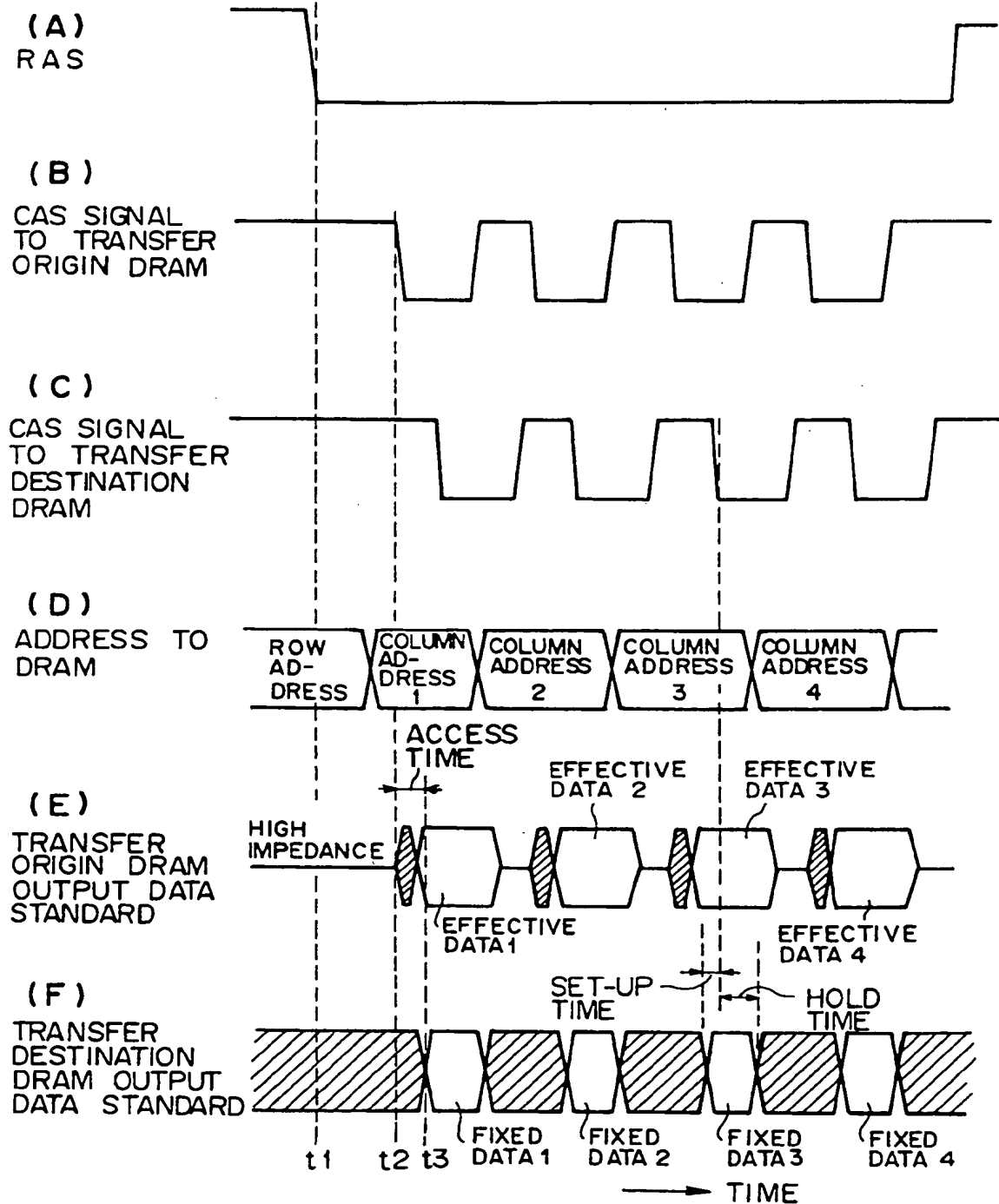
FIG. 3

FIG. 5

(A)
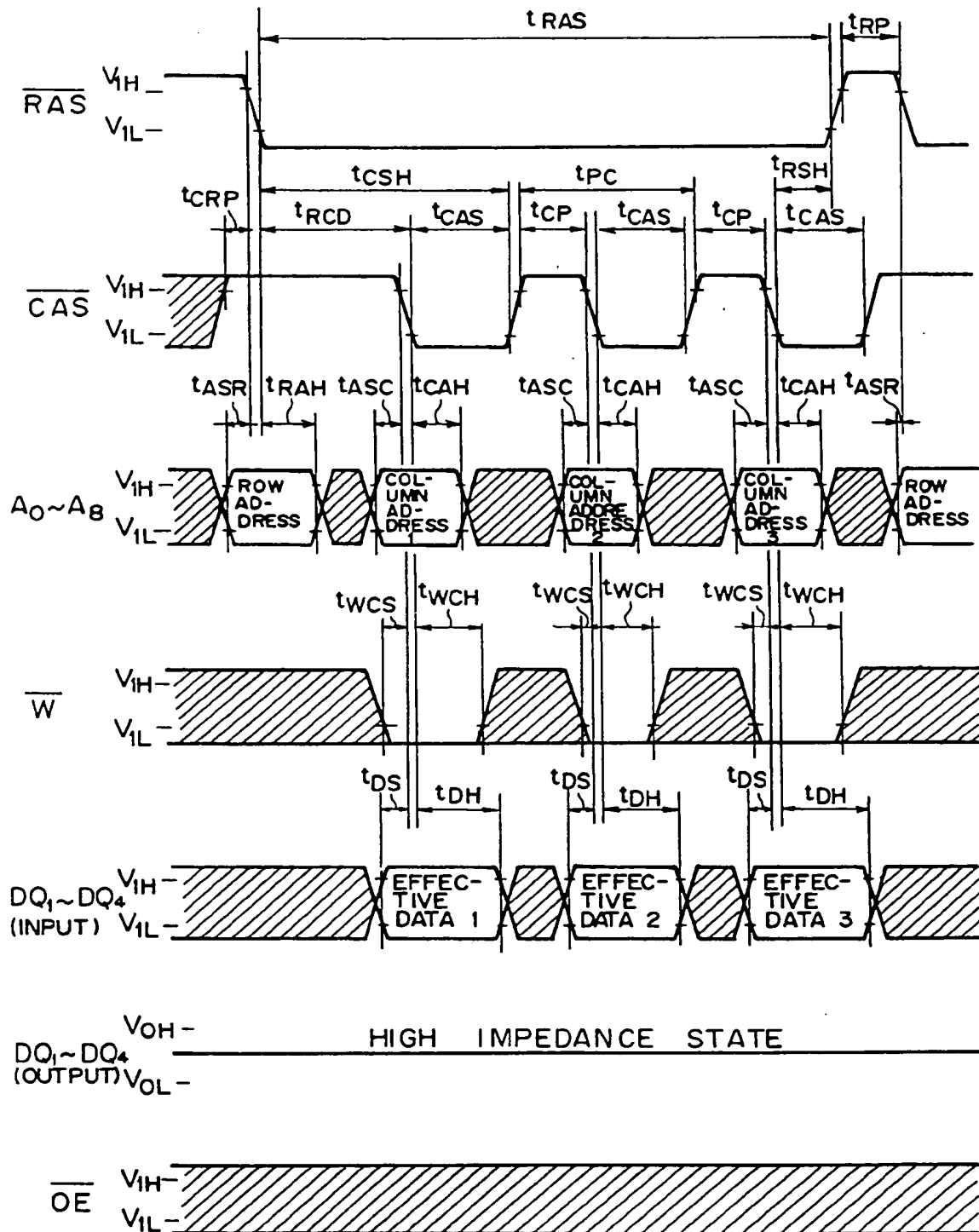R A S

(B)
CAS SIGNAL
TO TRANSFER
ORIGIN DRAM

(C)
CAS SIGNAL
TO TRANSFER
DESTINATION
DRAM

(D)
ADDRESS TO
DRAM

| ROW AD-DRESS | COLUMN AD-DRESS 1 | COLUMN ADDRESS 2 | COLUMN ADDRESS 3 | COLUMN ADDRESS 4 |

ACCESS TIME

(E)
TRANSFER
ORIGIN DRAM
OUTPUT DATA
STANDARD

HIGH IMPEDANCE

EFFECTIVE DATA 2   EFFECTIVE DATA 3

EFFECTIVE DATA 1   EFFECTIVE DATA 4

(F)
TRANSFER
DESTINATION
DRAM OUTPUT
DATA STANDARD

SET-UP TIME   HOLD TIME

FIXED DATA 1   FIXED DATA 2   FIXED DATA 3   FIXED DATA 4

t1   t2 t3

TIME

FIG. 7

FIG. 9